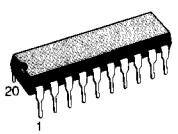
OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS

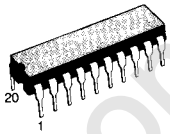
DESCRIPTION

The T54LS/T74LS240/241/244 are Octal Buffers and Line Drivers. These devices are designed to be used with 3-state memory address drivers, etc. They are organized as two lines of 4-bit with inverting or non-inverting data.

- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



B1
Plastic Package



D1/D2
Ceramic Package

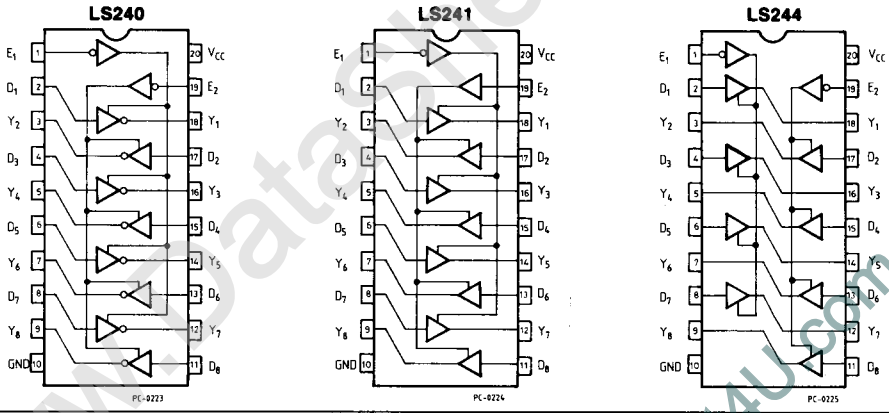
M1
Micro Package

C1
Plastic Chip Carrier

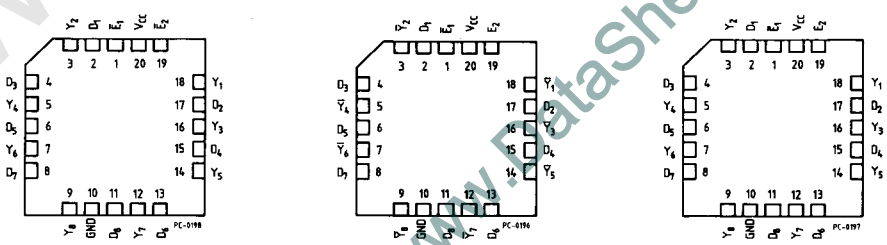
ORDERING NUMBERS:
T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

LOGIC DIAGRAMS AND PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

T54LS/T74LS240

INPUTS		OUTPUT
$\overline{E}_1$, $\overline{E}_2$	D	
L	L	H
L	H	L
H	X	(Z)

T54LS/T74LS244

INPUTS		OUTPUT
$\overline{E}_1$, $\overline{E}_2$	D	
L	L	L
L	H	H
H	X	(Z)

T54LS/T74LS241

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_1$	D		E_2	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = HIGH Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS240/241/244D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS240/241/244XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54,74	2.4	3.4		V_{CC} = MIN, I_{OH} = −3.0mA	V
		54,74	2.0			I_{OH} = −12mA for 54LS; I_{OH} = −15mA for 74LS; V_{CC} = MIN	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA; V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA	
V_{T+}-V_{T-}	Hysteresis		0.2	0.4		V_{CC} = MIN	V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V	μA
I_{IH}	Input HIGH Current				20	V_{CC} = MAX, V_{IN} = 2.7V	μA
					0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IL}	Input LOW Current				−0.2	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−40		−225	V_{CC} = MAX	mA
I_{CC}	Power Supply Current Total, Output HIGH				27	V_{CC} = MAX	mA
	Total, Out. LOW	LS240			44		
		LS241/244			46		
	Total at HIGH Z	LS240			50		
		LS241/244			54		

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_{PLH}	Propagation Delay,		9	14		ns
t_{PHL}	Data to Output LS240		12	18		
t_{PLH}	Propagation Delay, Data		12	18	C_L = 45pF	ns
t_{PHL}	to Output LS240/241/244		12	18	R_L = 667Ω	
t_{PZH}	Output Enable Time to HIGH Level		15	23		ns
t_{PZL}	Output Enable Time to LOW Level		20	30		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	C_L = 5.0pF	ns
t_{PHZ}	Output Disable Time from HIGH Level		10	18		ns

Notes:

1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC WAVEFORMS

Fig. 1

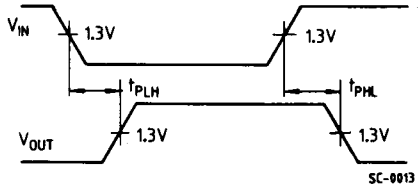


Fig. 2

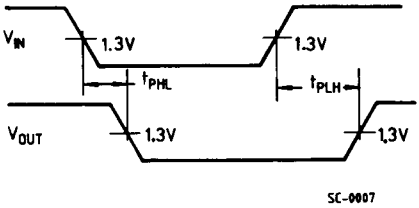


Fig. 3

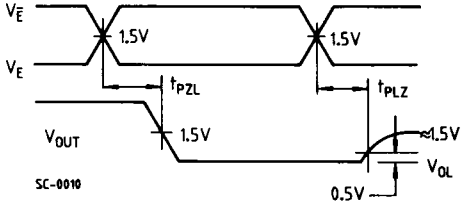


Fig. 4

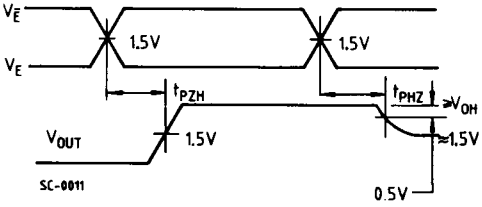
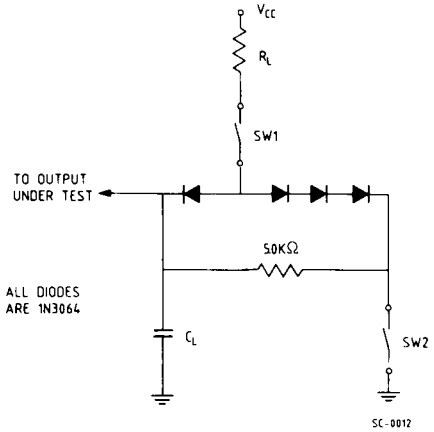


Fig. 5



SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed